REMARKS

Claims 1, 5, 8, 12, 26, 30, 33, and 37 are currently pending in the application.

This amendment is in response to the Final Rejection in the Office Action of February 18, 2003.

The drawings were objected to under 37 CFR 1.83(a). Applicant submits that drawing Fig.'s 3and 4 clearly describe the invention as set forth in the claims. Both drawing Fig.'s 3 and 4 illustrate in cross-section a semiconductor die 12 attached to a adapter board upper surface 20 of the adapter board 18 having a via 42 therein having, in turn, wires 134 extending therethrough. As drawing Fig.'s 3 and 4 illustrate the claimed invention in cross section, the views of the inventions illustrated therein are generic. As such, the inventions illustrated are representative of any cross section of any number of semiconductor die 12 mounted on an adapter board 18 having any number of vias 42 therethrough. Accordingly, Applicant submits that the drawings clearly comply with the provisions of 37 CFR 1.83(a).

Rejections Under 35 U.S.C. 112

Claims 1, 5, 8, 12, 26, 30, 33 and 37 are rejected under 35 U.S.C. § 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor, at the time the application was filed, had possession of the claimed invention. Applicant respectfully submits that the specification contains support for the phrase in Claim 1: "without any portion of the first substrate being located below the upper surface of the second substrate." Applicants invention relates to "an intermediate printed circuit board....that functions as an adaptor board for electrically connecting...bare semiconductor dies" to circuit boards which are not configured for direct attachment. Specification, pg. 5, lines 8-12. Such an adaptor is not limited to applications in which the adaptor is physically between the two elements electrically connected by it, and Applicant respectfully submits that Claim 1, in which the adaptor is positioned below the die and

other board element is a foreseeable embodiment of Applicant's invention. Claim 1 has been amended to more clearly claim this embodiment.

Furthermore, Applicant respectfully submits that the specification supports making explicit the inherent absence of recesses in the upper surfaces of specific board elements mentioned in the claims "for the location of semiconductor die." In Claims 5, 8, 12, 26, 30, 33 and 37, the board element to which the claim refers is in direct contact with another board element which separates it from the semiconductor die mentioned in the claim, and prevents its upper surface from coming into contact with any other die. Thus, Applicant clearly does not contemplate a recess for the die mentioned in the claim or any other die. Applicant submits that Claim 1, which is one specific embodiment of the general invention, the remaining embodiments of which inherently must involve boards without recesses, reasonably carries the same characteristic. Furthermore, Claim 1 requires that bond wire connections "extend[ing] between the die side surface of said second substrate and the die side surface of said first substrate." Thus, Applicant clearly does not contemplate a situation in which the board elements are in mutual contact, with a die in between, and therefore does not contemplate a board element with a recess.

Claims 1, 5, 8 through 11 and 33 through 36 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Of those, only Claims 1, 5, 11 and 33 are specifically addressed by the Examiner. The claims have been amended to remove the ambiguities. Applicant apologizes for the confusion. Please note that in Claim 26, it is intended that "said substrate" read "said *first* substrate," in contrast to Examiner's assumption.

Rejections under 35 U.S.C. 103 (a)

Claims 1 and 26 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eide (U.S. Patent 5,313,096) in view of Kohno et al. (U.S. Patent 5,293,068) and Lin et al. (U.S. Patent 5,239,198).

Claims 5, 6, 30, and 31 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eide in view of Lin.

Claims 8, 12, 33 and 37 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky (U.S. Patent 5,099,309) in view of Kohno et al. and Lin.

After carefully considering the cited prior art, the rejections, and the Examiner's comments, Applicant has amended the claimed invention where necessary to clearly distinguish over any combination of the cited prior art for any rejection under the provisions of 35 U.S.C. § 103.

The Supreme Court has established the standard of patentability to be applied in obviousness rejections in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966). This standard has been summarized in MPEP § 2141 into four factual inquires including "(A) determining of the scope and contents of the prior art; (B) ascertaining the differences between the prior art and the claims in issue; (C) resolving the level of ordinary skill in the pertinent art; and (D) evaluating evidence of secondary considerations." It should be noted that, when applying the required patentability standards of *Graham,* the basic considerations which apply to obviousness rejections based on 35 U.S.C. § 103 should include the following principles of patent law: "(A) the claimed invention must be considered as a whole; (B) the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination; (C) the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and (D) reasonable expectation of success is the standard with which obviousness is determined." *Hodosh v. Block Drug Co., Inc.*, 786 F.2d 1136, 1143 n.5, 229 USPQ 182, 187 n.5 (Fed. Cir. 1986).

Applicant further submits that to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Third, the cited prior art reference must teach or suggest all of the claim limitations. Furthermore, the suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on Applicant's disclosure.

With regard to Claims 1 and 26 which are rejected under 35 U.S.C. § 103(a) as being unpatentable over Eide in view of Kohno et al. and Lin et al., applicant respectfully submits that the Examiner is not met the requirements of points (B) and (C) at the end of the second preceding paragraph in her consideration of the references. Furthermore, the Examiner fails to establish a *prima facie* case of obviousness under 35 U.S.C. § 103 regarding the claimed invention.

In the Office Action it is argued that it would have been obvious to combine the method of semiconductor-to-board connection of Eide (Figure 10), modified by the axial bond placement of Kohno, with the board-to-board connection of Lin (Figure 4) to arrive at the claimed method of the invention.

First, Applicant again states an argument which was submitted two responses ago but remains unaddressed in any Office Action. When modifying one piece of prior art with another to arrive at the conclusion that the combination is obvious, "the proposed modification cannot render the prior art unsuitable for its intended purpose." MPEP 2104.01. The teaching or suggestion of Eide is to eliminate the waste of space among semiconductors attached to a substrate. Col. 1. lines 65-68, Col. 2 lines 1-2, lines 29-32. Eide specifically rejects the "outward" lead configuration of Fig. 9 in favor of his own "inward" lead configuration (Fig. 10) which "provides for substantially greater chip density within the chip stack." Col. 6, line 68. Taking the idea of axial bond placement from Kohno would inevitably lead to the space-inefficient "outward" lead configuration. Therefore the combination of Eide with Kohno is

improper and cannot establish a *prima facie* case of obviousness under 35 U.S.C. 103 because they teach away from any combination thereof and destroy the invention of Eide..

Second, "the references must suggest the desirability and thus the obviousness of making the combination. As set forth above, the combination of Eide and Kohno do not, let alone additionally teach their combination with Lin. Furthermore, Lin does not suggest its combination with the board-to-semiconductor attachment of Eide with or without the axial bond placement of Kohno.

Third, "the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention." As set forth above, Applicant's invention pertains to making an adaptor board which interconnects semiconductors and board elements. Lin does disclose a board-to-board connection, but it is only with the hindsight provided by Applicant's disclosure that the elements of the cited prior art are randomly picked and chosen for specific, relevant characteristics (connecting said second substrate to said first substrate having said second located solely on one side of said first substrate without any portion of said first substrate being located below said upper surface of said second substrate and portions of said plurality of bond wires extending between the second attachment surface of said second substrate and a surface of said first substrate, the connections between said first substrate and said second substrate formed by one of a plurality of solder balls and a plurality of pins) from the myriad of teachings or suggestions in Lin's Fig. 4.

For example, in Fig. 4, Lin also discloses putting traces on both sides of the second substrate. The two types of traces are electrically connected. Both types of traces are connected to the board. There are semiconductor die on both sides of the board. The die are packaged. The packaging occludes part of the surrounding traces. In short, it is from this complex picture that specific elements of the claimed invention are randomly picked and chosen and then combined with other teachings to reconstruct the claimed invention.

Fourth, nowhere in the Office Action is a *prima facie* case of obviousness under 35 U.S.C. 103 established meeting all the criteria as set forth herein. As set forth above, there is no

suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Claims 1 and 26 are allowable.

Claims 5, 6, 30, and 31 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Eide in view of Lin. Claims 6 and 31 were previously cancelled and are not pending in this application.

The second, third, and fourth arguments above are applicable with respect to such claims. Claims 5 and 30 are allowable.

Claims 8, 12, 33 and 37 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kryzaniwsky (U.S. Patent 5,099,309) in view of Kohno et al. and Lin. Applicant respectfully submits that the a *prima facie* case of obviousness under 35 U.S.C. § 103 has not been established regarding the claimed invention. With regard to Claims 8, 12, 33 and 37, there is no suggestion in any of the references to combine any two of them, let alone all three. Furthermore, as set forth above, it is impermissible hindsight to take the masterboard and electrical connections of Lin, while disregarding the remaining irrelevant elements, the presence of which, but for Applicant's disclosure, would have obscured the selection of the relevant elements. Applicant respectfully submits that Claims 8, 12, 33 and 37 are allowable.

ENTRY OF AMENDMENT

Applicant requests entry of this amendment for the following reasons:

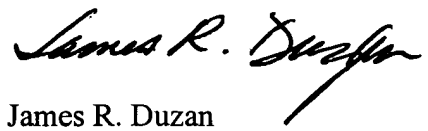
The amendment is timely filed.

The amendment places the application in condition for allowance.

The amendment does not require any further search or consideration .

In summary, for the reasons set forth herein, Applicants request the allowance of claims 1, 5, 8, 12, 26, 30, 33, and 37 and the case passed for issue.

Respectfully submitted,



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JRD/sls:djp

Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

A marked-up version of each of the presently amended claims, highlighting the changes thereto, follows:

1. (Four Times Amended) A method of electrically connecting a semiconductor die to a first substrate when said semiconductor die is attached to second substrate having an upper surface without recesses therein, comprising:

providing one of a semiconductor die having a surface having a plurality of bond pads extending along a longitudinal axis of said die on said surface and a semiconductor die having a surface having a plurality of bond pads extending in a leads-over-chip configuration on said surface;

providing a second substrate having a die side surface, a second attachment surface, at least one via extending through the substrate from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface and on the die side of the second substrate;

applying an adhesive to a portion of the die side of the first substrate to attach the semiconductor die thereto;

attaching the surface having a plurality of bond pads thereon of the semiconductor die to the die side surface of said second substrate so that the semiconductor die is located above the second substrate;

connecting said plurality of bond pads of the semiconductor die to said plurality of bond pads on the second attachment surface of said second substrate using a plurality of wire bonds, said plurality of wire bonds extending through said at least one via extending through said second substrate;

filling at least a portion of the via in the substrate with a sealant;

connecting said second substrate to said first substrate having said second located solely on one side of said first substrate without any portion of said first substrate being located below

said upper surface of said second substrate and portions of said plurality of bond wires extending between the [second attachment] die side surface of said second substrate and a die side surface of said first substrate, the connections between said first substrate and said second substrate formed by one of a plurality of solder balls and a plurality of pins.

5. (Twice Amended) A method of electrically connecting a semiconductor die to a master board, comprising:

providing a semiconductor die having a plurality of bond pads thereon;

providing a master board having a plurality of circuit traces on an upper surface thereof, said upper surface having no recesses therein;

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and a plurality of bond pads located on the second attachment surface of the board;

providing a plurality of electrical connectors for connecting the plurality of bond pads located on the second attachment surface of the board to the circuit traces of the master board;

attaching said semiconductor die to a portion of the die side surface of the board;

connecting said plurality of bond pads of said semiconductor die to said plurality of bond pads of said board using a plurality of wire bonds, said plurality of wire bonds extending through the [at least one via]plurality of vias extending through then board; and

connecting said board and master board using said plurality of electrical connectors on said board to said plurality of circuit traces on said master board using one of a plurality of solder balls and a plurality of pins, said board being located above the upper surface of said master board.

26. (Four Times Amended) A method of attaching a semiconductor die to a first substrate for attaching said first substrate to a second substrate having an upper surface free of recesses for semiconductor die and having a plurality of circuit traces thereon, comprising:

providing one of a semiconductor die having a surface having at least one bond pad located along a longitudinal axis of said die on said surface and a semiconductor die having a surface having at least one bond pad extending in a leads-over configuration on said surface;

providing a first substrate having a die side surface, a second attachment surface, at least one via extending through the board from the die side surface to the second attachment surface, a plurality of circuits, and at least one bond pad located on the second attachment surface of the first substrate;

filling a potion of the via in the substrate with a sealant

applying an adhesive to a portion of the die side of the substrate to attach the semiconductor die thereto;

attaching the surface having at least one bond pad thereon of the semiconductor die to the die side surface of said first substrate;

connecting said at least one bond pad of the semiconductor die to said at least one bond pad of said first substrate using at least one wire bond, said at least one wire bond extending through said at least one via extending through said substrate; and

attaching said first substrate to said upper surface of said second substrate using one of a plurality of solder balls and a plurality of pins.

30. (Three Times Amended) A method of attaching a semiconductor die to a master board, comprising:

providing a semiconductor die having at least one bond pad thereon;

providing a master board having at least one circuit trace on an upper surface thereof, said upper surface free of any recess for the receipt of a semiconductor die therein;

providing a board having a die side surface, a second attachment surface, a plurality of vias extending through the board from the die side surface to the second attachment surface, at least one circuit, and at least one bond pad located on the second attachment surface of the board;

providing at least one electrical connector for connecting the at least one bond pad located on the second attachment surface of the board to the at least one circuit trace of the master board;

attaching said semiconductor die to a portion of the die side surface of the board;

connecting said at least one bond pad of said semiconductor die to said at least one bond pad of said board using at least one wire bond, said at least one wire bond extending through the [at least one via] plurality of vias extending through [then] the board; and

connecting said board and master board using said at least one electrical connector on said board to said at least one circuit trace on said master board using at least one of at least one solder ball and at least one pin as a connector.